Refine Search

Search Results -

Terms	Documents
L1 same first same second	34

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Search History

DATE: Tuesday, May 17, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same first same second	34	L2
L1	DMA near10 ASIC	314	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
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Database:
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US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, May 17, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same first same second	34	L2
L1	DMA near10 ASIC	314	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
(709/208 |709/212 |710/22 |710/300 |710/308 |710/72 |710/74 |710/240 |710/241 |710/113 |711/100 |711/202).ccls.	6469

Database:
- US Pre-Grant Publication Full-Text Database
- US Patents Full-Text Database
- US OCR Full-Text Database
- EPO Abstracts Database
- JPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L1

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, May 17, 2005 Printable Copy Create Case

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DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L1	710/22,300,308,72,74,240,241,113;711/100,202;709/208,212.ccls.	6469	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L1 and L2	32

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L3

Refine Search

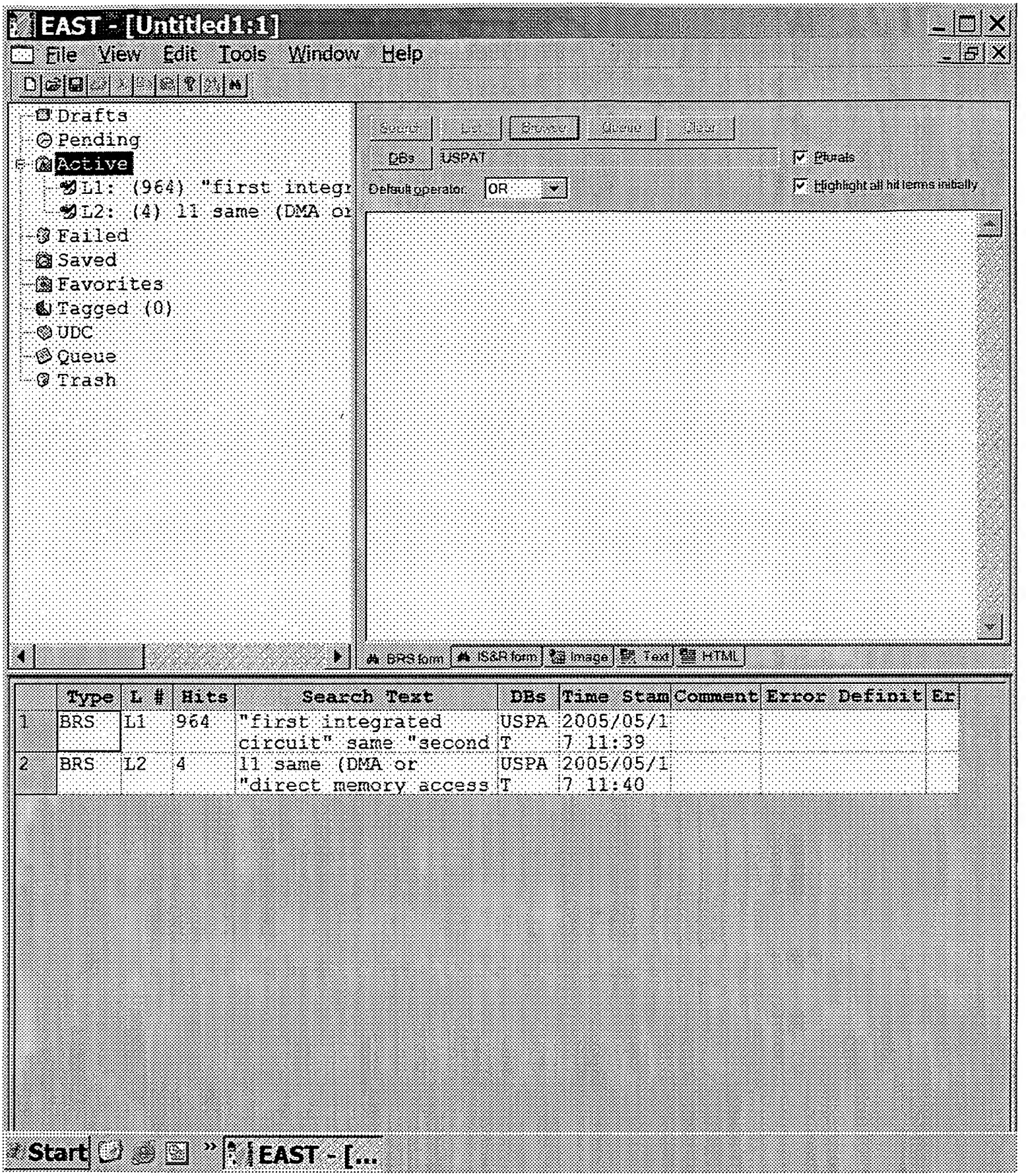
Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, May 17, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L3	l1 and L2	32	L3
L2	DMA near10 ASIC	314	L2
L1	710/22,300,308,72,74,240,241,113;711/100,202;709/208,212.ccls.	6469	L1

END OF SEARCH HISTORY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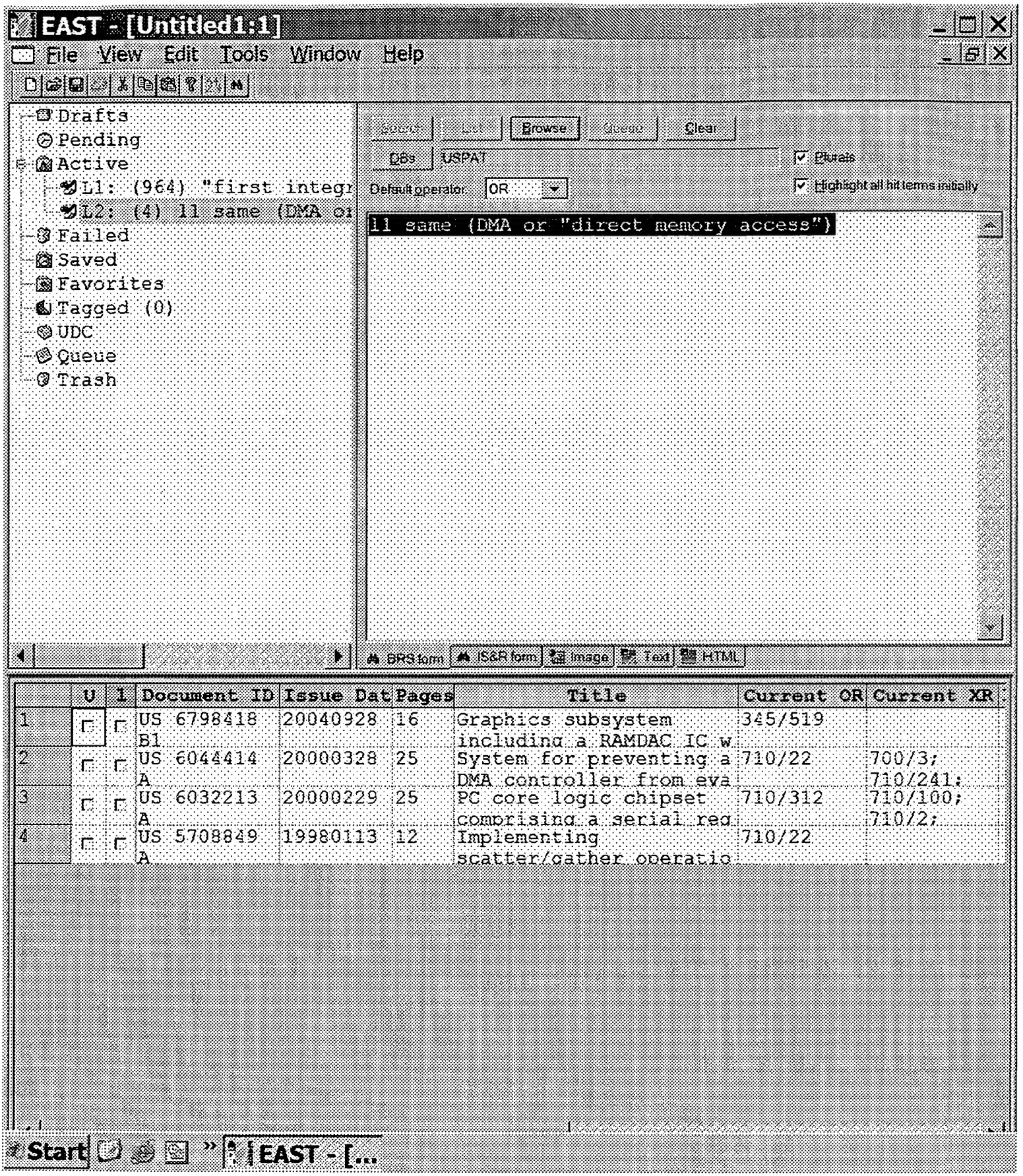
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1
US 6798418 B1
20040928
16
Graphics subsystem including a RAMDAC IC w
345/519
2
US 6044414 A
20000328
25
System for preventing a DMA controller from eva
710/22
700/3; 710/241;
3
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20000229
25
PC core logic chipset comprising a serial req
710/312
710/100; 710/2;
4
US 5708849 A
19980113
12
Implementing scatter/gather operatio
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Start
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Results for "(dma<in>metadata) <and> (asic<in>metadata)"

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(dma<in>metadata) <and> (asic<in>metadata)

Check to search only within this results set

Display Format: Citation Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

Select Article Information

1. **ASIC design in a next generation workstation**
Young, M.S.;
ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE
17-21 Sept. 1990 Page(s):P2/6.1 - P2/6.4
AbstractPlus | Full Text: PDF(276 KB) IEEE CNF

2. **An ASIC RISC-based I/O processor for computer applications**
Cates, R.L.; Farrell, J.J., III;
Euro ASIC '90
29 May-1 June 1990 Page(s):50 - 55
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3. **A floating point convolution system**
Panisset, J.F.; Drolet, J.; Cote, J.F.; Larochelle, F.; Malowany, A.S.;
Circuits and Systems, 1990., Proceedings of the 33rd Midwest Symposium on
12-14 Aug. 1990 Page(s):397 - 400 vol.1
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4. **Thoughts on core integration and test**
Anderson, T.L.;
Test Conference, 1997. Proceedings., International
1-6 Nov. 1997 Page(s):1039
AbstractPlus | Full Text: PDF(96 KB) IEEE CNF

5. **Design and implementation of an ATM segmentation engine with PCI interface**
Chan Kim; Jong-Arm Jun; Kyou-Ho Lee; Hyup-Jong Kim;
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Volume 6, 31 May-3 June 1998 Page(s):510 - 513 vol.6
AbstractPlus | Full Text: PDF(376 KB) IEEE CNF

6. **ASIC design of a microcontroller with power management unit**
Seung-Il Sonh; Hun-Mo Yang; Jong-Ick Lee; Moon-Key Lee;
Semiconductor Conference, 1998. CAS '98 Proceedings. 1998 International
Volume 1, 6-10 Oct. 1998 Page(s):159 - 162 vol.1
AbstractPlus | Full Text: PDF(352 KB) IEEE CNF

7. **Control and communication performance analysis of embedded DSP systems in the MASIC methodology**
Deb, A.K.; Oberg, J.; Jantsch, A.;
System Synthesis, 2001. Proceedings. The 14th International Symposium on
2001 Page(s):274 - 279

AbstractPlus | Full Text: PDF(1120 KB) IEEE CNF

8. **Design of a multichip module containing a 12 Way S/390 microprocessor subsystem**
Kohler, H.;
ASIC Conference and Exhibit, 1996. Proceedings., Ninth Annual IEEE International
23-27 Sept. 1996 Page(s):187 - 190
AbstractPlus | Full Text: PDF(336 KB) IEEE CNF

9. **Design and verification of an embedded microprocessor**
Onufryk, P.Z.;
Industrial Technology, 1996. (ICIT '96), Proceedings of The IEEE International Conference on
2-6 Dec. 1996 Page(s):786 - 790
AbstractPlus | Full Text: PDF(584 KB) IEEE CNF

10. **The APIC approach to high performance network interface design: protected DMA and other techniques**
Dittia, Z.D.; Parulkar, G.M.; Cox, J.R., Jr.;
INFOCOM '97. Sixteenth Annual Joint Conference of the IEEE Computer and Communications Societies. Proceedings IEEE
Volume 2, 7-11 April 1997 Page(s):823 - 831 vol.2
AbstractPlus | Full Text: PDF(1268 KB) IEEE CNF

11. **The ManArray™ embedded processor architecture**
Pechanek, G.G.; Vassiliadis, S.;
Euromicro Conference, 2000. Proceedings of the 26th
Volume 1, 5-7 Sept. 2000 Page(s):348 - 355 vol.1
AbstractPlus | Full Text: PDF(548 KB) IEEE CNF

12. **Embedded DRAM built in self test and methodology for test insertion**
Jakobsen, P.; Dreibelbis, J.; Pomichter, G.; Anand, D.; Barth, J.; Nelms, M.; Leach, J.; Belansek, G.;
Test Conference, 2001. Proceedings. International
30 Oct.-1 Nov. 2001 Page(s):975 - 984
AbstractPlus | Full Text: PDF(571 KB) IEEE CNF

ASIC design in a next generation workstation

Young, M.S.
Sun Microsystems Inc., Mountain View, CA, USA;

This paper appears in: **ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE**
Publication Date: 17-21 Sept. 1990
On page(s): P2/6.1 - P2/6.4
Meeting Date: 09/17/1990 - 09/21/1990
Location: Rochester, NY
INSPEC Accession Number:4111835
DOI: 10.1109/ASIC.1990.186100
Posted online: 2002-08-06 17:34:54.0

Abstract
The activities of the design team formed for development of a follow-on machine to the Sparcstation 1 are discussed. The design team partitioned the design into four chips: the cache controller (CACHE+), memory management unit (MMU+), direct memory access (**DMA+**), and dynamic memory controller (RAM+). Architectural changes and higher integration eliminated two of the ASICs used on the Sparcstation 1 and dropped the usage of one of the ASICs from two to one part per board. One **ASIC**, a video controller, was reused. The manpower requirements of the project and the design/verification tools used by the design team are discussed

Index Terms
Inspec

Controlled Indexing
CMOS integrated circuits VLSI application specific integrated circuits buffer storage circuit CAD design engineering file organisation storage management chips workstations

Non-controlled Indexing
ASIC design CACHE+ **DMA+** MMU+ RAM+ cache controller design/verification tools direct memory access dynamic memory controller follow-on machine higher integration manpower requirements memory management unit new Sparcstation next generation workstation video controller

Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

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Design and verification of an embedded microprocessor

Onufryk, P.Z.
AT&T Bell Labs. Res., Murray Hill, NJ, USA;

This paper appears in: **Industrial Technology, 1996. (ICIT '96), Proceedings of The IEEE International Conference on**
Publication Date: 2-6 Dec. 1996
On page(s): 786 - 790
Number of Pages: xvi+884
Meeting Date: 12/02/1996 - 12/06/1996
Location: Shanghai
INSPEC Accession Number:5623104
DOI: 10.1109/ICIT.1996.601705
Posted online: 2002-08-06 20:20:06.0

Abstract
Advances in VLSI technologies are enabling the construction of entire systems on a chip. A major challenge in the design of such systems is design verification. This paper presents the design and verification process used to develop Euphony. Euphony is an inexpensive low power system on a chip which contains: a RISC processor with DSP functions, a complex memory and device controller, two ATM network interfaces, architectural support for AAL5 SAR processing, a five channel **DMA** controller, and a serial port that can interface to wide variety of audio devices. Euphony was developed jointly by AT&T and LSI Logic. AT&T developed the architecture while LSI Logic performed the implementation using LSI Logic's LCB500K 0.5 micron drawn cell-based **ASIC** processes. Both companies were heavily involved in design verification

Index Terms
Inspec

Controlled Indexing
VLSI asynchronous transfer mode computer testing digital signal processing chips integrated circuit design integrated circuit testing logic CAD real-time systems reduced instruction set computing

Non-controlled Indexing
AAL5 SAR processing AT& T ATM network interfaces DMA controller DSP functions Euphony LSI Logic RISC processor VLSI embedded microprocessor function verification signal processing system on chip

Author Keywords
Not Available

References

No references available on IEEE Xplore.

Citing Documents

No citing documents available on IEEE Xplore.

View Search Results | Previous Article | Next Article

L2: Entry 27 of 34 File: USPT Dec 17, 1996

DOCUMENT-IDENTIFIER: US 5586291 A
TITLE: Disk controller with volatile and non-volatile cache memories

Detailed Description Text (26):
Cache memory control circuit 40 may be provided as a cache memory control application specific integrated circuit (ASIC) which controls both the SIMMs 32' and the NVSIMMs 34'. It is understood that although cache memory control circuit 40 is here described as a single ASIC in some embodiments it may be desirable to provided control circuit 40 as two or more separate ASICs. For example a first ASIC could direct address control and a second different ASIC could direct data and error control. Suffice it to say that the cache memory control circuit 40 may perform a variety of control functions including but not limited to cache control and DMA control and that each of such functions may be performed by one or more ASICs. For example, a DMA ASIC could control DMA transfers between the NVSIMMs and the volatile SIMMs.

L2: Entry 27 of 34 File: USPT Dec 17, 1996

US-PAT-NO: 5586291
DOCUMENT-IDENTIFIER: US 5586291 A

TITLE: Disk controller with volatile and non-volatile cache memories

DATE-ISSUED: December 17, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lasker; Jeffrey M.	Marlboro	MA		
McGillis; James M.	Franklin	MA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
EMC Corporation	Hopkinton	MA			02

APPL-NO: 08/ 363298 [PALM]
DATE FILED: December 23, 1994

INT-CL: [06] G06 F 13/00

US-CL-ISSUED: 395/440; 395/492
US-CL-CURRENT: 711/113; 711/165

FIELD-OF-SEARCH: 395/440, 395/492, 395/842, 395/873, 395/876

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4392200	July 1983	Arulpragasam et al.	395/467
☐	4439829	March 1984	Tsiang	395/445
☐	4755930	July 1988	Wilson, Jr. et al.	395/449
☐	4794524	December 1988	Carberry et al.	395/375
☐	4831581	May 1989	Rubinfeld	395/250
☐	4885680	December 1989	Anthony et al.	364/471
☐	4888689	December 1989	Taylor et al.	364/467
☐	4899275	February 1990	Sachs et al.	364/403
☐	4972338	November 1990	Crawford et al.	364/416
☐	4985829	January 1991	Thatte et al.	364/417

☐	5067078	November 1991	Talgam et al.	395/403
☐	5073851	December 1991	Masterson et al.	395/467
☐	5091846	February 1992	Sachs et al.	395/250
☐	5107457	April 1992	Hayes et al.	395/800
☐	5146571	September 1992	Logan	395/182.06
☐	5150472	September 1992	Blank et al.	395/464
☐	5151989	September 1992	Johnson et al.	395/600
☐	5163142	November 1992	Mageau	395/469
☐	5170476	December 1992	Laakso et al.	395/467
☐	5193166	March 1993	Menasce	395/447
☐	5257352	October 1993	Yamamoto et al.	395/463
☐	5274787	December 1993	Hirano et al.	395/470
☐	5276833	January 1994	Auvinen et al.	395/432
☐	5287473	February 1994	Mohan et al.	395/460
☐	5303362	April 1994	Butts, Jr. et al.	395/448
☐	5347642	September 1994	Barratt	395/440
☐	5349651	September 1984	Hetherington et al.	395/417

ART-UNIT: 238

PRIMARY-EXAMINER: Robertson; David L.

ATTY-AGENT-FIRM: Weingarten, Schurgin, Gagnebin & Hayes LLP

ABSTRACT:

A disk storage subsystem includes both volatile and non-volatile portions of memory. In response to a write command from a host computer, the controller allocates a predetermined number of memory blocks in the non-volatile cache memory and allocates a corresponding number of blocks in the volatile memory. Host supplied write data is then stored in the allocated non-volatile memory blocks. The data may also be mirrored in additional non-volatile memory. Immediately thereafter the subsystem sends an acknowledge signal to the host. The subsystem then performs a DMA operation to copy the write-data from the non-volatile memory blocks to the volatile memory blocks. The write-data is then stored on a disk drive at which point the non-volatile memory may be de-allocated. Subsequent reads of the given data may be read from the volatile memory, reducing disk access time. In the event of a power failure, data stored in the non-volatile memory but not yet written to disk is preserved. In the event of a disk controller failure, the non-volatile memory modules may be transferred to a functioning disk controller for recovery.

23 Claims, 9 Drawing figures

Previous Doc Next Doc Go to Doc#

L2: Entry 26 of 34 File: USPT Sep 1, 1998

DOCUMENT-IDENTIFIER: US 5802327 A
TITLE: Device for SCSI expansion

Detailed Description Text (15):
DMA controller 216 is coupled to first SCSI bus 208 and second SCSI bus 209. DMA controller 216 can be an ASIC or other circuitry or device. DMA controller 216 can be a single chip or can comprise a plurality of chips. DMA controller 216 is coupled to SCSI bus 208 and SCSI bus 209. DMA controller 216 allows DMA data transfer between a first SCSI peripheral coupled to first SCSI bus 208 and a computer system coupled to second SCSI bus 209. A DMA file transfer can be accomplished by transmitting a starting address from the computer system on SCSI bus 209 for the data transfer, transmitting byte count information for the data transfer and transmitting the data. Likewise, a DMA data transfer can be accomplished in the other direction by transmitting a starting address from the SCSI device on SCSI bus 208, transmitting byte count information for the data transfer and transmitting the data.

L2: Entry 26 of 34 File: USPT Sep 1, 1998

US-PAT-NO: 5802327
DOCUMENT-IDENTIFIER: US 5802327 A

TITLE: Device for SCSI expansion

DATE-ISSUED: September 1, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hawley; Brian N.	Riverside	CA		
Saunders; Michael C.	Riverside	CA		
Tolsma; Arthur R.	Redlands	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Luminex Software Incorporated	Riverside	CA			02

APPL-NO: 08/ 558961 [PALM]
DATE FILED: November 13, 1995

INT-CL: [06] G06 F 1/00

US-CL-ISSUED: 395/281; 395/822, 395/823, 395/308
US-CL-CURRENT: 710/300; 710/2, 710/3

FIELD-OF-SEARCH: 395/281, 395/842, 395/306, 395/308, 395/822, 395/823

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5202979	April 1993	Hillis et al.	395/575
☐	5239632	August 1993	Larner	395/325
☐	5274783	December 1993	House et al.	395/325
☐	5564026	October 1996	Amini et al.	395/308

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CDM-4000 Quad-Speed CD Mastering System Data Specification, Dynatek Structured For Storage, 2 pps., (Nov. 1994).
CD Studio Specification Document, Young Minds, Inc., 4 pps., (1994).

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Pancholi; Jigar

ATTY-AGENT-FIRM: Blakely Sokoloff Taylor & Zafman

ABSTRACT:

A SCSI expansion device receives a first SCSI identifier and logical unit number from a first SCSI bus for identifying a first SCSI peripheral. The SCSI expansion device converts the first SCSI identifier and logical unit number to a second SCSI identifier and logical unit number and represents the first SCSI peripheral to external devices coupled to a second SCSI bus with the second SCSI identifier and logical unit number.

15 Claims, 11 Drawing figures

Previous Doc Next Doc Go to Doc#

L2: Entry 17 of 34 File: USPT Mar 16, 2004

DOCUMENT-IDENTIFIER: US 6708285 B2
TITLE: Redundant controller data storage system having system and method for handling controller resets

Detailed Description Text (10):
In one preferred embodiment, the task processor 52 operates to copy the memory image of first mirrored memory 50 to second memory 56 while the system operation processor 54 continues to process system operation commands. As such, hot insertion of the second controller 34 into the redundant controller system 30 does not result in undo delay to the processing of system operation commands and/or a timeout by a host system via host system interface 42. In one exemplary embodiment, task processor 52 performs background tasks without direct involvement of system operation processor 54 or other system processors, via specialized data processing hardware. In one aspect, the data processing hardware is coupled to an intelligent DMA engine, as part of an application specific integrated circuit (ASIC). Task processor 52 has the ability to process specific background tasks during continued operation of the first controller 32 via system operation processor 50. In one aspect, task processor 52 operates to perform a memory-to-memory copy task, a memory self-test, as well as other tasks.

L2: Entry 17 of 34 File: USPT Mar 16, 2004

US-PAT-NO: 6708285
DOCUMENT-IDENTIFIER: US 6708285 B2

TITLE: Redundant controller data storage system having system and method for handling controller resets

DATE-ISSUED: March 16, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Oldfield; Barry J.	Boise	ID		
Johansson; Christopher W.	Horseshoe Bend	ID		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hewlett-Packard Development Company, L.P.	Houston	TX			02

APPL-NO: 09/ 810108 [PALM]
DATE FILED: March 15, 2001

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This Non-Provisional Patent Application is related to commonly assigned U.S. patent application Ser. No. 09/810,103, filed on Mar. 15, 2001, entitled "Redundant Controller Data Storage System Having On-Line Controller Removal System and Method," which is incorporated herein by reference; and U.S. patent application Ser. No. 09/810,102, filed on Mar. 15, 2001, entitled "Redundant Controller Data Storage System Having Fast Insertion System and Method," which is incorporated herein by reference.

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/11
US-CL-CURRENT: 714/11

FIELD-OF-SEARCH: 714/6, 714/7, 714/8, 714/9, 714/11, 714/12, 714/23, 714/24, 710/302

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4958273	September 1990	Anderson et al.	
☐	5155835	October 1992	Belsan	
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☐	5274645	December 1993	Idleman et al.	
☐	5278838	January 1994	Ng et al.	
☐	5287462	February 1994	Jibbe et al.	
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☐	5495570	February 1996	Heugel et al.	
☐	5546539	August 1996	Poling	
☐	5553230	September 1996	Petersen et al.	
☐	5568641	October 1996	Nelson et al.	
☐	5574863	November 1996	Nelson et al.	
☐	5666512	September 1997	Nelson et al.	
☐	5682471	October 1997	Billings et al.	
☐	5699510	December 1997	Petersen et al.	
☐	5856989	January 1999	Oldfield et al.	
☐	5915082	June 1999	Marshall et al.	714/11
☐	5928367	July 1999	Nelson et al.	
☐	5960451	September 1999	Voigt et al.	
☐	6085332	July 2000	El-Batal	
☐	6092168	July 2000	Voigt	
☐	6138247	October 2000	McKay et al.	714/10
☐	6327675	December 2001	Burdett et al.	714/11

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
4364514	December 1992	JP	

ART-UNIT: 2184

PRIMARY-EXAMINER: Beausoliel; Robert

ASSISTANT-EXAMINER: Bonzo; Bryce P.

ABSTRACT:

A redundant controller data storage system having a system and method for handling controller resets is described. In one aspect, the method of handling a controller reset in a redundant controller system according to the present invention includes the redundant controller system having a first controller and a second controller. A controller reset is detected on the second controller. The first controller is notified of the controller reset via a communication link between the first controller and the second controller. A shutdown process on the first controller and the second controller is performed. The communication link between the first controller and the second controller is disabled, wherein detection of a subsequent controller reset via the second controller cannot be communicated to the first controller via the communication link.

17 Claims, 13 Drawing figures

Previous Doc Next Doc Go to Doc#

Refine Search

Search Results -

Terms	Documents
DMA same (first adj1 (IC or "integrated circuit")) same (second adj1 (IC or "integrated circuit"))	7

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L5

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, May 17, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L5	DMA same (first adj1 (IC or "integrated circuit")) same (second adj1 (IC or "integrated circuit"))	7	L5
L4	DMA same (first adj1 ASIC) same (second adj1 ASIC)	0	L4
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same first same second	34	L2
L1	DMA near10 ASIC	314	L1

END OF SEARCH HISTORY

Refine Search

Search Results -

Terms	Documents
L5	0

Database:
US Pre-Grant Publication Full-Text Database
US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Search: L6

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Tuesday, May 17, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L6	L5	0	L6
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L5	DMA same (first adj1 (IC or "integrated circuit")) same (second adj1 (IC or "integrated circuit"))	7	L5
L4	DMA same (first adj1 ASIC) same (second adj1 ASIC)	0	L4
DB=EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L3	L2	0	L3
DB=PGPB,USPT,USOC; PLUR=YES; OP=OR			
L2	L1 same first same second	34	L2
L1	DMA near10 ASIC	314	L1

END OF SEARCH HISTORY

L5: Entry 4 of 7 File: USPT Sep 28, 2004

DOCUMENT-IDENTIFIER: US 6798418 B1
TITLE: Graphics subsystem including a RAMDAC IC with digital video storage interface for connection to a graphics bus

Brief Summary Text (15):
In one embodiment, a graphics processor implemented on a first integrated circuit chip is configured to render digital image information in response to graphics commands and to store the digital image information in a memory. The graphics commands may be received, for example, from a main CPU within a computer system associated with the graphics subsystem. A conversion unit is further provided on a second integrated circuit chip, which includes a color mapping unit and a digital-to-analog converter. The color mapping unit may include a RAM look-up table and is configured to convert the digital image information into digital RGB display data. The digital-to-analog converter is coupled to convert the digital RGB display data into one or more analog signals for driving a video display. The graphics subsystem further includes a Direct Memory Access (DMA) controller implemented on the second integrated circuit chip. The DMA controller is configured to generate read requests to retrieve the digital image information stored in the memory and to thereby cause the digital image information to be provided to the conversion unit. The DMA controller is further configured to generate write cycles to cause the digital RGB display data to be written to a designated region of memory. The operating system may then transfer the digital RGB display data from the memory into a storage device such as a hard disk drive.

CLAIMS:

1. A graphics subsystem comprising: a graphics processor implemented on a first integrated circuit chip, wherein said graphics processor is configured to render digital image information in response to a graphics command received from a CPU and to store said digital image information in a memory; a conversion unit implemented on a second integrated circuit chip, wherein said conversion unit includes a color mapping unit coupled to convert said digital image information to digital RGB display data, wherein said conversion unit further includes a digital-to-analog converter coupled to convert said digital RGB display data to one or more analog signals for driving a video display; and a DMA controller implemented on said second integrated circuit chip, wherein said DMA controller is configured to generate read requests to retrieve said digital image information stored in said memory and to cause said digital image information to be provided to said conversion unit; wherein said DMA controller is further configured to generate write cycles to cause said digital RGB display data to be written to a designated memory region.

18. A computer system comprising: a CPU; a graphics subsystem coupled to said CPU including: a graphics processor implemented on a first integrated circuit chip, wherein said graphics processor is configured to render digital image information in response to a graphics command received from said CPU and to store said digital image information in a first memory; a conversion unit implemented on a second integrated circuit chip, wherein said conversion unit includes a color mapping unit coupled to convert said digital image information to digital RGB display data, wherein said conversion unit further includes a digital-to-analog converter coupled to convert said digital RGB display data to one or more analog signals for driving a video display; and a DMA controller implemented on said second integrated circuit chip, wherein said DMA controller is configured to generate read requests to retrieve said digital image information stored in said first memory and to cause said digital image information to be provided to said conversion unit; wherein said DMA controller is further configured to generate write cycles to cause said digital RGB display data to be written to a designated memory region.

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L5: Entry 4 of 7 File: USPT Sep 28, 2004

US-PAT-NO: 6798418
DOCUMENT-IDENTIFIER: US 6798418 B1

TITLE: Graphics subsystem including a RAMDAC IC with digital video storage interface for connection to a graphics bus

DATE-ISSUED: September 28, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sartori; Gabriele	Fremont	CA		
Gulick; Dale E.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 577527 [PALM]
DATE FILED: May 24, 2000

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 345/519
US-CL-CURRENT: 345/519

FIELD-OF-SEARCH: 375/240, 375/240.27, 345/509, 345/643, 345/519, 345/506, 345/558, 345/420, 345/419, 345/501, 345/522, 345/520, 326/38, 710/26, 710/312, 710/305, 710/200, 710/56, 710/22, 710/52, 701/208, 711/147, 370/263

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5099331	March 1992	Truong	
☐	5798770	August 1998	Baldwin	
☐	5821918	October 1998	Reinert et al.	345/643
☐	6008821	December 1999	Bright et al.	
☐	6020901	February 2000	Lavelle et al.	345/509
☐	6091778	July 2000	Sporer et al.	375/240
☐	6145025	November 2000	Lim	710/22
☐	6201834	March 2001	Zhu	375/240.27

☐	6219725	April 2001	Diehl et al.	710/26
☐	6433579	August 2002	Wang et al.	326/38
☐	6442477	August 2002	Okada	701/208

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
WO 97/39437	October 1997	WO	
WO 00/28518	May 2000	WO	

OTHER PUBLICATIONS

Specification for ADV478/ADV471, Analog Devices, Inc., pp. 1-12.

ART-UNIT: 2676

PRIMARY-EXAMINER: Bella; Matthew C.

ASSISTANT-EXAMINER: Singh; Dalip K.

ATTY-AGENT-FIRM: Meyertons Hood Kivlin Kower & Goetzel, P.C. Kivlin; B. Noel Curran; Stephen J.

ABSTRACT:

A graphics subsystem including a RAMDAC for connection to a graphics bus implemented on an integrated circuit chip separate from a graphics processor. In one embodiment, the graphics processor is configured to render digital image information in response to graphics commands and to store the digital image information in a memory. The RAMDAC IC includes a conversion unit, which includes a color mapping unit and a digital-to-analog converter and is configured to convert a representation of the digital image information into one or more analog signals for driving a video display. The graphics subsystem further includes a Direct Memory Access (DMA) controller implemented on the second integrated circuit chip. The DMA controller is configured to generate read requests to retrieve the digital image information stored in the memory to thereby cause the digital image information to be provided to the conversion unit. The DMA controller is further configured to generate write cycles to cause digital RGB display data received from the color mapping unit, in the conversion unit, to be provided for storage in a specified region of memory. In another embodiment, the graphics subsystem may include a digital video interface implemented on the second integrated circuit chip. The digital video interface is configured to receive digital RGB display data from the color mapping unit and to provide an encoded digital video output to a digital video output port. The digital video interface is further configured to receive encoded digital video from a digital video input port and to provide decoded digital display data for storage on devices such as a digital VCR.

36 Claims, 9 Drawing figures

Previous Doc Next Doc Go to Doc#

L5: Entry 5 of 7 File: USPT Mar 28, 2000

DOCUMENT-IDENTIFIER: US 6044414 A
TITLE: System for preventing a DMA controller from evaluating its DRQ input once a DMA operation has started until the DRQ input has been updated

Abstract Text (1):
A computer system includes first and second integrated circuits. A direct memory access (DMA) controller circuit on the first integrated circuit receives a direct memory access request (DRQ) input signal which is provided from the second integrated circuit, across a signal line of said bus. The value of the DRQ signal is updated at predetermined intervals on the signal line. A DMA synchronization control circuit on the first integrated circuit prevents the DMA controller circuit from evaluating its DRQ input signal, once a DMA operation has started, until after the value of the DRQ input signal has been updated by the second integrated circuit. In addition, the DMA acknowledge signal from the DMA controller circuit is mapped to an address indicative of the acknowledge signal, and the address is sent to the second integrated circuit. A decoder circuit on the second integrated circuit decodes the address and provides the appropriate DMA acknowledge signal to a functional block on the second integrated circuit according to the address received.

Brief Summary Text (15):
One problem associated with such a solution is to ensure that direct memory access information provided to the first integrated circuit is valid. Because of the inherent delay of a serial bus, such information may be invalid when the DMA control circuit expects the information to be valid. Accordingly, the present invention provides a computer system including a first and second integrated circuits which are coupled by a serial bus. A direct memory access (DMA) circuit is on the first integrated circuit and coupled to receive a direct memory access request (DRQ) input signal from the second integrated circuit. The value of the DRQ signal is provided from said second integrated circuit, across a signal line of the bus with the value being updated periodically the signal line;

Brief Summary Text (16):
Accordingly, a DMA synchronization control circuit on the first integrated circuit, prevents the DMA circuit from evaluating its DRQ input signal until after the DRQ input signal has been updated by said second integrated circuit after a DMA operation. In addition, the DMA acknowledge signal from the DMA controller circuit is mapped to an address indicative of the acknowledge signal, and the address is sent to the second integrated circuit. A decoder circuit on the second integrated circuit decodes the address and provides the appropriate DMA acknowledge signal according to the address received.

CLAIMS:

1. A computer system including a first and a second integrated circuit, coupled by a bus, comprising:

a direct memory access (DMA) controller circuit disposed on said first integrated circuit and coupled to receive a direct memory access (DMA) request (DRQ) signal, a value of said DRQ signal being provided from said second integrated circuit, across a signal line of said bus, said value being updated at a predetermined interval on said signal line;

a DMA synchronization control circuit disposed on said first integrated circuit, said DMA synchronization control circuit preventing said DMA controller circuit from evaluating said DRQ signal until after said DRQ signal has been updated by said second integrated circuit after a DMA operation has completed.

4. The computer system as recited in claim 3, wherein said DMA controller circuit disposed on said first integrated circuit is responsive to a first and a second DMA request signal to provide respectively a first and second DMA acknowledge signal, and wherein said first integrated circuit further includes an address circuit coupled to receive said first and second DMA request signals, said address circuit for mapping said first DMA acknowledge signal to a first address and the second DMA acknowledge signal to a second address, said first integrated circuit coupled to selectably provide one of said first and second addresses to said second integrated circuit across said bus according to which of said first and second DMA acknowledge signals is asserted.

13. A method of operating a computer system including a first and a second integrated circuit, coupled by a bus, comprising:

providing from said second integrated circuit, across a signal line of said bus, an asserted direct memory access (DMA) request indication to said first integrated circuit, thereby indicating that a functional circuit block on said second integrated circuit is requesting a direct memory access (DMA) operation;

providing said asserted direct memory access request indication to a direct memory request (DRQ) input of a direct memory access (DMA) controller circuit disposed on said first integrated circuit;

after a start of a DMA operation responsive to said asserted DMA request indication, prohibiting said direct memory access controller circuit from evaluating said DRQ input until after said functional circuit block has received control information related to said direct memory access operation and has provided said direct memory access circuit with an updated direct memory access request indication in response.

17. A method for operating a computer system including a first and a second integrated circuit coupled by a bus, said first integrated circuit including a direct memory access (DMA) controller circuit receiving a first direct memory access request (DRQ) signal, said second integrated circuit including a first functional block receiving a local direct memory access acknowledge signal and providing a direct memory access request signal;

sending said direct memory access request (DRQ) signal, provided from said first functional block on said second integrated circuit to said DMA controller circuit on said first integrated circuit over a signal line of said bus;

providing a DMA acknowledge signal, as part of a DMA operation responsive to said DRQ signal, from said DMA controller circuit to an address circuit on said first functional block;

mapping said DMA acknowledge signal to an address corresponding to said DMA acknowledge signal; and

sending said address to said second integrated circuit.

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L5: Entry 5 of 7 File: USPT Mar 28, 2000

US-PAT-NO: 6044414
DOCUMENT-IDENTIFIER: US 6044414 A

TITLE: System for preventing a DMA controller from evaluating its DRQ input once a DMA operation has started until the DRQ input has been updated

DATE-ISSUED: March 28, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gulick; Dale E.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyavle	CA			02

APPL-NO: 09/ 024293 [PALM]
DATE FILED: February 17, 1998

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application relates to the following co-pending application entitled "PC CORE LOGIC SERIAL REGISTER ACCESS BUS", Ser. No. 08/928,035, still pending filed Sep. 11, 1997, by Dale E. Gulick; which application is incorporated herein by reference.

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 710/22; 710/241, 710/266, 364/132
US-CL-CURRENT: 710/22; 700/3, 710/241, 710/266

FIELD-OF-SEARCH: 710/21, 710/22, 710/113, 710/241, 710/260, 364/132

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4663730	May 1987	Ikeda	364/140
☐	4683530	July 1987	Quatse	364/200
☐	5373493	December 1994	Iizuka	369/124
☐	5410542	April 1995	Gerbehy et al.	370/85.1
☐	5450591	September 1995	Palmer	710/113
☐	5740387	April 1998	Lambrecht et al.	395/309

☐	5778252	July 1998	Sangveraphunsiri et al.	710/21
☐	5835733	November 1998	Walsh et al.	395/281
☐	5894578	April 1999	Qureshi et al.	710/266
☐	5941976	August 1999	Gulick	710/260

OTHER PUBLICATIONS

Intel, "82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator", May 1996, pp. 1-118.
Common Architecture, "Desktop PC/AT systems", Mar. 21, 1996, Version .93 Preliminary, pp. 1-26.

Advanced Micro Devices, "AM7968/Am7969 TAXIchip.TM. Article Reprints", Jan. 22, 1987, pp. 1-77, particularly pp. 67-72.
National Semiconductor, "PC87306 SuperI/O.TM. Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UART's, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface", Preliminary--Nov. 1995, pp. 1-110.
Shanley and Anderson, "ISA System Architecture", MindShare Press, Richardson, TX, 1991 and 1993, pp. 367-388.
Messmer, "The Indispensable PC Hardware Book--Your Hardware Questions Answered Second Edition", Addison Wesley Longman Limited, Harlow England, 1995, pp. 598-621.
Intel, "Low Pin Count (LPC) Interface Specification", Revision 1.0, Intel Corporation, 1997, pp. 1-31.
Harris Semiconductor, "CMOS High Performance Programmable DMA Controller", Harris Corporation, Mar. 1997, pp. 4-192 to 4-214.

ART-UNIT: 272

PRIMARY-EXAMINER: Lee; Thomas C.

ASSISTANT-EXAMINER: Elamin; Abdelmoniem

ATTY-AGENT-FIRM: Zagorin, O'Brien & Graham, LLP

ABSTRACT:

A computer system includes first and second integrated circuits. A direct memory access (DMA) controller circuit on the first integrated circuit receives a direct memory access request (DRQ) input signal which is provided from the second integrated circuit, across a signal line of said bus. The value of the DRQ signal is updated at predetermined intervals on the signal line. A DMA synchronization control circuit on the first integrated circuit prevents the DMA controller circuit from evaluating its DRQ input signal, once a DMA operation has started, until after the value of the DRQ input signal has been updated by the second integrated circuit. In addition, the DMA acknowledge signal from the DMA controller circuit is mapped to an address indicative of the acknowledge signal, and the address is sent to the second integrated circuit. A decoder circuit on the second integrated circuit decodes the address and provides the appropriate DMA acknowledge signal to a functional block on the second integrated circuit according to the address received.

23 Claims, 17 Drawing figures

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L5: Entry 6 of 7 File: USPT Feb 29, 2000

DOCUMENT-IDENTIFIER: US 6032213 A
** See image for Certificate of Correction **
TITLE: PC core logic chipset comprising a serial register access bus

CLAIMS:

26. The method as recited in claim 17 further comprising providing to a DMA request line at least one DMA request bit, said one DMA request bit indicating a state of a DMA request from a first functional block in the second integrated circuit to a DMA controller on the first integrated circuit.

L5: Entry 6 of 7 File: USPT Feb 29, 2000

US-PAT-NO: 6032213
DOCUMENT-IDENTIFIER: US 6032213 A
**** See image for Certificate of Correction ****

TITLE: PC core logic chipset comprising a serial register access bus

DATE-ISSUED: February 29, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gulick; Dale E.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 08/ 928035 [PALM]
DATE FILED: September 11, 1997

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application relates to the following applications: Ser. No. 08/802,321, filed Feb. 18, 1997, entitled "SYSTEM FOR PARTITIONING PC CHIPSET FUNCTIONS INTO LOGIC AND PORT INTEGRATED CIRCUITS", by Dale E. Gulick; Ser. No. 08/802,323, now U.S. Pat. No. 5,926,629, filed Feb. 18, 1997, entitled "CONTINUOUSLY OPERATING INTERCONNECTION BUS", by Dale E. Gulick; Ser. No. 08/928,034, filed the same day as the present application, entitled "PC CHIPSET WITH USER CONFIGURABLE PROGRAMMABLE LOGIC STRUCTURE", by Dale E. Gulick; and Ser. No. 08/929,153, filed the same day as the present application, entitled "SYSTEM POWER MANAGEMENT PARTITIONED ACROSS A SERIAL BUS", by Dale E. Gulick; all of which applications are incorporated herein by reference.

INT-CL: [07] G06 F 13/00, G06 F 13/42

US-CL-ISSUED: 710/129; 710/2, 710/22, 710/28, 710/100, 710/126, 710/260, 710/266, 712/38, 713/502
US-CL-CURRENT: 710/312; 710/100, 710/2, 710/22, 710/260, 710/266, 710/28, 712/38, 713/502

FIELD-OF-SEARCH: 710/101, 710/129, 710/130, 710/2, 710/28, 710/100, 710/260, 710/266, 710/48, 710/22, 710/61, 710/126, 710/105, 710/106, 712/38, 712/40, 713/400, 713/502

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4683530	July 1987	Quatse	710/2
☐	4885538	December 1989	Hoenniger, III et al.	324/312

☐	5410542	April 1995	Gerbehy et al.	370/85.1
☐	5634069	May 1997	Hicok et al.	710/33
☐	5740387	April 1998	Lambrecht et al.	710/129
☐	5778199	July 1998	Wanner et al.	710/107
☐	5790831	August 1998	Lin et al.	395/500
☐	5799208	August 1998	Hwang et al.	710/38
☐	5822548	October 1998	Story et al.	710/106
☐	5822554	October 1998	Conway	710/129
☐	5833733	November 1998	Walsh et al.	710/101
☐	5841631	November 1998	Shin et al.	361/684
☐	5941976	August 1999	Gulick	710/260

OTHER PUBLICATIONS

Intel, "82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator", May 1996, pp. 1-118.
Common Architecture, "Desktop PC/AT systems", Mar. 21, 1996, Version .93 Preliminary, pp. 1-26.

Advanced Micro Devices, "AM7968/Am7969 TAXIchip.TM. Article Reprints", Jan. 22, 1987, pp. 1-77, particularly pp. 67-72.
National Semiconductor, "PC87306 SuperI/O.TM. Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface", Preliminary-Nov. 1995, pp. 1-110.

ART-UNIT: 271

PRIMARY-EXAMINER: Thai; Xuan M.

ATTY-AGENT-FIRM: Zagorin, O'Brien & Graham, LLP

ABSTRACT:

A computer system includes first and second integrated circuits. The first integrated circuit provides a first input/output bus operating in accordance with a first protocol, such as ISA. The first input/output bus includes a plurality of address and data lines respectively providing address and data information. The second integrated circuit includes a plurality of second functional blocks at least some of which interface to legacy devices. The first integrated circuit includes a host controller circuit, coupled to the first input/output bus and for coupling to a register access bus which includes a register data out and a register data in signal line. The register access bus connects the first and second integrated circuits. The host controller circuit receives address and data information from the input/output bus and serially provides the address and data information to the data out line. A target controller circuit on the second integrated circuit is coupled to the register access bus. The target controller circuit receives the serially provided address and data information and provides the address and data information, over a second representation of the input/output bus, the second representation being at least a subset of the first protocol and including a plurality of internal address lines and a plurality of internal data lines coupled to the second functional blocks. Write operations take place to memory locations in the second integrated circuit from a write operation begun on the first integrated circuit and read operations take place from memory locations in the second integrated circuit for read operations begun on the first integrated circuit.

36 Claims, 15 Drawing figures

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L5: Entry 6 of 7 File: USPT Feb 29, 2000

US-PAT-NO: 6032213
DOCUMENT-IDENTIFIER: US 6032213 A
**** See image for Certificate of Correction ****

TITLE: PC core logic chipset comprising a serial register access bus

DATE-ISSUED: February 29, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Gulick; Dale E.	Austin	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advanced Micro Devices, Inc.	Sunnyvale	CA			02

APPL-NO: 08/ 928035 [PALM]
DATE FILED: September 11, 1997

PARENT-CASE:
CROSS REFERENCE TO RELATED APPLICATIONS This application relates to the following applications: Ser. No. 08/802,321, filed Feb. 18, 1997, entitled "SYSTEM FOR PARTITIONING PC CHIPSET FUNCTIONS INTO LOGIC AND PORT INTEGRATED CIRCUITS", by Dale E. Gulick; Ser. No. 08/802,323, now U.S. Pat. No. 5,926,629, filed Feb. 18, 1997, entitled "CONTINUOUSLY OPERATING INTERCONNECTION BUS", by Dale E. Gulick; Ser. No. 08/928,034, filed the same day as the present application, entitled "PC CHIPSET WITH USER CONFIGURABLE PROGRAMMABLE LOGIC STRUCTURE", by Dale E. Gulick; and Ser. No. 08/929,153, filed the same day as the present application, entitled "SYSTEM POWER MANAGEMENT PARTITIONED ACROSS A SERIAL BUS", by Dale E. Gulick; all of which applications are incorporated herein by reference.

INT-CL: [07] G06 F 13/00, G06 F 13/42

US-CL-ISSUED: 710/129; 710/2, 710/22, 710/28, 710/100, 710/126, 710/260, 710/266, 712/38, 713/502
US-CL-CURRENT: 710/312; 710/100, 710/2, 710/22, 710/260, 710/266, 710/28, 712/38, 713/502

FIELD-OF-SEARCH: 710/101, 710/129, 710/130, 710/2, 710/28, 710/100, 710/260, 710/266, 710/48, 710/22, 710/61, 710/126, 710/105, 710/106, 712/38, 712/40, 713/400, 713/502

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4683530	July 1987	Quatse	710/2
☐	4885538	December 1989	Hoenniger, III et al.	324/312

☐	5410542	April 1995	Gerbehy et al.	370/85.1
☐	5634069	May 1997	Hicok et al.	710/33
☐	5740387	April 1998	Lambrecht et al.	710/129
☐	5778199	July 1998	Wanner et al.	710/107
☐	5790831	August 1998	Lin et al.	395/500
☐	5799208	August 1998	Hwang et al.	710/38
☐	5822548	October 1998	Story et al.	710/106
☐	5822554	October 1998	Conway	710/129
☐	5833733	November 1998	Walsh et al.	710/101
☐	5841631	November 1998	Shin et al.	361/684
☐	5941976	August 1999	Gulick	710/260

OTHER PUBLICATIONS

Intel, "82371FB (PIIX) and 82371SB (PIIX3) PCI ISA IDE Xcelerator", May 1996, pp. 1-118.
Common Architecture, "Desktop PC/AT systems", Mar. 21, 1996, Version .93 Preliminary, pp. 1-26.

Advanced Micro Devices, "AM7968/Am7969 TAXIchip.TM. Article Reprints", Jan. 22, 1987, pp. 1-77, particularly pp. 67-72.
National Semiconductor, "PC87306 SuperI/O.TM. Enhanced Sidewinder Lite Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, Infrared Interface, IEEE 1284 Parallel Port, and IDE Interface", Preliminary-Nov. 1995, pp. 1-110.

ART-UNIT: 271

PRIMARY-EXAMINER: Thai; Xuan M.

ATTY-AGENT-FIRM: Zagorin, O'Brien & Graham, LLP

ABSTRACT:

A computer system includes first and second integrated circuits. The first integrated circuit provides a first input/output bus operating in accordance with a first protocol, such as ISA. The first input/output bus includes a plurality of address and data lines respectively providing address and data information. The second integrated circuit includes a plurality of second functional blocks at least some of which interface to legacy devices. The first integrated circuit includes a host controller circuit, coupled to the first input/output bus and for coupling to a register access bus which includes a register data out and a register data in signal line. The register access bus connects the first and second integrated circuits. The host controller circuit receives address and data information from the input/output bus and serially provides the address and data information to the data out line. A target controller circuit on the second integrated circuit is coupled to the register access bus. The target controller circuit receives the serially provided address and data information and provides the address and data information, over a second representation of the input/output bus, the second representation being at least a subset of the first protocol and including a plurality of internal address lines and a plurality of internal data lines coupled to the second functional blocks. Write operations take place to memory locations in the second integrated circuit from a write operation begun on the first integrated circuit and read operations take place from memory locations in the second integrated circuit for read operations begun on the first integrated circuit.

36 Claims, 15 Drawing figures

Previous Doc Next Doc Go to Doc#

L5: Entry 7 of 7 File: USPT Jan 13, 1998

DOCUMENT-IDENTIFIER: US 5708849 A
TITLE: Implementing scatter/gather operations in a direct memory access device on a personal computer

Detailed Description Text (7):
Also connected to the PCI bus 12 is a PCI/secondary bus bridge circuit 17. The bridge circuit 17 performs the various functions necessary to transfer data between the PCI bus 12 and various component circuits joined to a secondary bus 18. The secondary bus 18 may be an ISA bus or a EISA bus both of which transfer data at rates slower than does the bus 12. One specific PCI to EISA bus bridge circuit 17 is a part of a chip set manufactured by Intel Corporation and referred to as the 82374EB and 82375EB-EISA Bridge. Such a bridge circuit is described in detail in a publication by Intel Corporation entitled 82420/82430 PCIset, ISA and EISA Bridges. Such a bridge circuit 17 includes circuitry for providing the interfaces between the PCI bus 12 and the secondary bus 18 so that data may be transferred therebetween. The bridge circuit 17 is manufactured in one embodiment as a two chip integrated circuit set; a first one of these integrated circuits performs functions related to the PCI bus 12 and a second one of these integrated circuits performs functions related to the secondary (EISA) bus 18. The first integrated circuit provides circuitry which allows the bridge 17 to operate as an intercoupling bus master or a bus slave on the PCI bus 12. The second integrated circuit includes circuitry which allows the bridge 17 to perform bus master or bus slave functions on the secondary (EISA) bus 18. The bridge circuit 17 also includes within the two integrated circuit chips a first arbiter circuit 20 for controlling access to the PCI bus 12 and a second arbiter circuit 21 for controlling access to the secondary bus 18. In one embodiment, the circuitry of the EISA control portion of the bridge circuit 17 includes a DMA device connected as a bus master on the secondary bus 18 which is adapted to provide the advantages of the present invention. The ability of the bridge circuit 17 to act as a PCI bus master and a secondary bus slave allows a bus master circuit 19 positioned on the secondary bus 18 (for example, the DMA circuitry) to gain access to the PCI bus 12 and thence to the main memory. The PCI agents 16 may also gain access to component devices on the secondary bus in a similar manner.

L5: Entry 7 of 7 File: USPT Jan 13, 1998

US-PAT-NO: 5708849
DOCUMENT-IDENTIFIER: US 5708849 A

TITLE: Implementing scatter/gather operations in a direct memory access device on a personal computer

DATE-ISSUED: January 13, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Coke; James S.	Cameron Park	CA		
Bhatt; Ajay V.	Eldorado Hills	CA		
Graham; Stan	Cameron Park	CA		
Lent; David	Placerville	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 791008 [PALM]
DATE FILED: January 27, 1997

PARENT-CASE:
This is a continuation of application Ser. No. 08/187,751, filed Jan. 26, 1994, now abandoned.

INT-CL: [06] G06 F 13/10

US-CL-ISSUED: 395/842; 395/310
US-CL-CURRENT: 710/22

FIELD-OF-SEARCH: 395/842, 395/843, 395/844, 395/845, 395/846, 395/847, 395/848, 395/310

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5155830	October 1992	Kurashige	395/844
☐	5175825	December 1992	Starr	395/425
☐	5182800	January 1993	Farrell et al.	395/844
☐	5212795	May 1993	Hendry	395/848
☐	5251303	October 1993	Fogg, Jr. et al.	395/844

☐	5291582	March 1994	Drako et al.	395/425
☐	5333290	July 1994	Kato	395/846
☐	5333294	July 1994	Schnell	395/846
☐	5367639	November 1994	Sodos	395/844

ART-UNIT: 232

PRIMARY-EXAMINER: Chan; Eddie P.

ASSISTANT-EXAMINER: Nguyen; Hiep T.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A direct memory access (DMA) circuit includes a first register for storing an address for the transfer of data, apparatus for transferring data at sequential addresses beginning at the address in the first register until all data at sequential addresses has been transferred, a second register for storing a beginning address for a list of addresses, and a state machine which responds to the completion of a transfer of data at sequential addresses beginning at the address in the first register and an indication that more data is to be transferred to transfer an address from the list at the address in the second register to the first register and causes the apparatus for transferring data to commence.

19 Claims, 6 Drawing figures

Previous Doc Next Doc Go to Doc#

L5: Entry 7 of 7 File: USPT Jan 13, 1998

US-PAT-NO: 5708849
DOCUMENT-IDENTIFIER: US 5708849 A

TITLE: Implementing scatter/gather operations in a direct memory access device on a personal computer

DATE-ISSUED: January 13, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Coke; James S.	Cameron Park	CA		
Bhatt; Ajay V.	Eldorado Hills	CA		
Graham; Stan	Cameron Park	CA		
Lent; David	Placerville	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA			02

APPL-NO: 08/ 791008 [PALM]
DATE FILED: January 27, 1997

PARENT-CASE:
This is a continuation of application Ser. No. 08/187,751, filed Jan. 26, 1994, now abandoned.

INT-CL: [06] G06 F 13/10

US-CL-ISSUED: 395/842; 395/310
US-CL-CURRENT: 710/22

FIELD-OF-SEARCH: 395/842, 395/843, 395/844, 395/845, 395/846, 395/847, 395/848, 395/310

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5155830	October 1992	Kurashige	395/844
☐	5175825	December 1992	Starr	395/425
☐	5182800	January 1993	Farrell et al.	395/844
☐	5212795	May 1993	Hendry	395/848
☐	5251303	October 1993	Fogg, Jr. et al.	395/844

☐	5291582	March 1994	Drako et al.	395/425
☐	5333290	July 1994	Kato	395/846
☐	5333294	July 1994	Schnell	395/846
☐	5367639	November 1994	Sodos	395/844

ART-UNIT: 232

PRIMARY-EXAMINER: Chan; Eddie P.

ASSISTANT-EXAMINER: Nguyen; Hiep T.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor & Zafman

ABSTRACT:

A direct memory access (DMA) circuit includes a first register for storing an address for the transfer of data, apparatus for transferring data at sequential addresses beginning at the address in the first register until all data at sequential addresses has been transferred, a second register for storing a beginning address for a list of addresses, and a state machine which responds to the completion of a transfer of data at sequential addresses beginning at the address in the first register and an indication that more data is to be transferred to transfer an address from the list at the address in the second register to the first register and causes the apparatus for transferring data to commence.

19 Claims, 6 Drawing figures

Previous Doc Next Doc Go to Doc#

US006798418B1

(12) **United States Patent**
Sartori et al.

(10) **Patent No.: US 6,798,418 B1**
(45) **Date of Patent: Sep. 28, 2004**

(54) **GRAPHICS SUBSYSTEM INCLUDING A RAMDAC IC WITH DIGITAL VIDEO STORAGE INTERFACE FOR CONNECTION TO A GRAPHICS BUS**

(75) Inventors: **Gabriele Sartori**, Fremont, CA (US); **Dale E. Gulick**, Austin, TX (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/577,527**

(22) Filed: **May 24, 2000**

(51) **Int. Cl.**[7] **G06F 13/14**

(52) **U.S. Cl.** **345/519**

(58) **Field of Search** 375/240, 240.27; 345/509, 643, 519, 506, 558, 420, 419, 501, 522, 520; 326/38; 710/26, 312, 305, 200, 56, 22, 52; 701/206; 711/147; 370/263

(56) **References Cited**

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6,442,477	B1	*	8/2002	Okada 701/208

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WO	WO 00/28518		5/2000

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* cited by examiner

Primary Examiner—Matthew C. Bella
Assistant Examiner—Dalip K. Singh
(74) *Attorney, Agent, or Firm*—Meyertons Hood Kivlin Kowert & Goetzel, P.C.; B. Noël Kivlin; Stephen J. Curran

(57) **ABSTRACT**

A graphics subsystem including a RAMDAC for connection to a graphics bus implemented on an integrated circuit chip separate from a graphics processor. In one embodiment, the graphics processor is configured to render digital image information in response to graphics commands and to store the digital image information in a memory. The RAMDAC IC includes a conversion unit, which includes a color mapping unit and a digital-to-analog converter and is configured to convert a representation of the digital image information into one or more analog signals for driving a video display. The graphics subsystem further includes a Direct Memory Access (DMA) controller implemented on the second integrated circuit chip. The DMA controller is configured to generate read requests to retrieve the digital image information stored in the memory to thereby cause the digital image information to be provided to the conversion unit. The DMA controller is further configured to generate write cycles to cause digital RGB display data received from the color mapping unit, in the conversion unit, to be provided for storage in a specified region of memory. In another embodiment, the graphics subsystem may include a digital video interface implemented on the second integrated circuit chip. The digital video interface is configured to receive digital RGB display data from the color mapping unit and to provide an encoded digital video output to a digital video output port. The digital video interface is further configured to receive encoded digital video from a digital video input port and to provide decoded digital display data for storage on devices such as a digital VCR.

36 Claims, 9 Drawing Sheets

100

US-PAT-NO: 6798418

DOCUMENT-IDENTIFIER: US 6798418 B1

TITLE: Graphics subsystem including a RAMDAC IC with digital video storage interface for connection to a graphics bus

---------- KWIC ----------

Brief Summary Text - BSTX (15):

In one embodiment, a graphics processor implemented on a first integrated circuit chip is configured to render digital image information in response to graphics commands and to store the digital image information in a memory. The graphics commands may be received, for example, from a main CPU within a computer system associated with the graphics subsystem. A conversion unit is further provided on a second integrated circuit chip, which includes a color mapping unit and a digital-to-analog converter. The color mapping unit may include a RAM look-up table and is configured to convert the digital image information into digital RGB display data. The digital-to-analog converter is coupled to convert the digital RGB display data into one or more analog signals for driving a video display. The graphics subsystem further includes a Direct Memory Access (DMA) controller implemented on the second integrated circuit chip. The DMA controller is configured to generate read requests to retrieve the digital image information stored in the memory and to thereby cause the digital image information to be provided to the conversion unit. The DMA controller is further configured to generate write cycles to cause the digital RGB display data to be written to a designated region of memory. The operating system may then transfer the digital RGB display data from the memory into a storage device such as a hard disk drive.

Claims Text - CLTX (1):

1. A graphics subsystem comprising: a graphics processor implemented on a first integrated circuit chip, wherein said graphics processor is configured to render digital image information in response to a graphics command received from a CPU and to store said digital image information in a memory; a conversion unit implemented on a second integrated circuit chip, wherein said conversion unit includes a color mapping unit coupled to convert said digital image information to digital RGB display data, wherein said conversion unit further includes a digital-to-analog converter coupled to convert said digital RGB display data to one or more analog signals for driving a video display; and a DMA controller implemented on said second integrated circuit chip, wherein said DMA controller is configured to generate read requests to retrieve said digital image information stored in said memory and to cause said digital image information to be provided to said conversion unit; wherein said DMA controller is further configured to generate write cycles to cause said digital RGB display data to be written to a designated memory region.

Claims Text - CLTX (18):

US006044414A

United States Patent [19]

Gulick

[11] Patent Number: 6,044,414

[45] Date of Patent: Mar. 28, 2000

[54] **SYSTEM FOR PREVENTING A DMA CONTROLLER FROM EVALUATING ITS DRQ INPUT ONCE A DMA OPERATION HAS STARTED UNTIL THE DRQ INPUT HAS BEEN UPDATED**

[75] Inventor: **Dale E. Gulick**, Austin, Tex.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: 09/024,293

[22] Filed: Feb. 17, 1998

[51] Int. Cl.[7] G06F 13/14

[52] U.S. Cl. 710/22; 710/241; 710/266; 364/132

[58] Field of Search 710/21, 22, 113, 710/241, 260; 364/132

[56] **References Cited**

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Primary Examiner—Thomas C. Lee
Assistant Examiner—Abdelmoniem Elamin
Attorney, Agent, or Firm—Zagorin, O'Brien & Graham, LLP

[57] **ABSTRACT**

A computer system includes first and second integrated circuits. A direct memory access (DMA) controller circuit on the first integrated circuit receives a direct memory access request (DRQ) input signal which is provided from the second integrated circuit, across a signal line of said bus. The value of the DRQ signal is updated at predetermined intervals on the signal line. A DMA synchronization control circuit on the first integrated circuit prevents the DMA controller circuit from evaluating its DRQ input signal, once a DMA operation has started, until after the value of the DRQ input signal has been updated by the second integrated circuit. In addition, the DMA acknowledge signal from the DMA controller circuit is mapped to an address indicative of the acknowledge signal, and the address is sent to the second integrated circuit. A decoder circuit on the second integrated circuit decodes the address and provides the appropriate DMA acknowledge signal to a functional block on the second integrated circuit according to the address received.

23 Claims, 14 Drawing Sheets

US-PAT-NO: 6044414

DOCUMENT-IDENTIFIER: US 6044414 A

TITLE: System for preventing a DMA controller from evaluating its DRQ input once a DMA operation has started until the DRQ input has been updated

---------- KWIC ---------

Abstract Text - ABTX (1):

A computer system includes first and second integrated circuits. A direct memory access (DMA) controller circuit on the first integrated circuit receives a direct memory access request (DRQ) input signal which is provided from the second integrated circuit, across a signal line of said bus. The value of the DRQ signal is updated at predetermined intervals on the signal line. A DMA synchronization control circuit on the first integrated circuit prevents the DMA controller circuit from evaluating its DRQ input signal, once a DMA operation has started, until after the value of the DRQ input signal has been updated by the second integrated circuit. In addition, the DMA acknowledge signal from the DMA controller circuit is mapped to an address indicative of the acknowledge signal, and the address is sent to the second integrated circuit. A decoder circuit on the second integrated circuit decodes the address and provides the appropriate DMA acknowledge signal to a functional block on the second integrated circuit according to the address received.

Brief Summary Text - BSTX (15):

One problem associated with such a solution is to ensure that direct memory access information provided to the first integrated circuit is valid. Because of the inherent delay of a serial bus, such information may be invalid when the DMA control circuit expects the information to be valid. Accordingly, the present invention provides a computer system including a first and second integrated circuits which are coupled by a serial bus. A direct memory access (DMA) circuit is on the first integrated circuit and coupled to receive a direct memory access request (DRQ) input signal from the second integrated circuit. The value of the DRQ signal is provided from said second integrated circuit, across a signal line of the bus with the value being updated periodically the signal line;

Brief Summary Text - BSTX (16):

Accordingly, a DMA synchronization control circuit on the first integrated circuit, prevents the DMA circuit from evaluating its DRQ input signal until after the DRQ input signal has been updated by said second integrated circuit after a DMA operation. In addition, the DMA acknowledge signal from the DMA controller circuit is mapped to an address indicative of the acknowledge signal, and the address is sent to the second integrated circuit. A decoder circuit on the second integrated circuit decodes the address and provides the appropriate DMA acknowledge signal according to the address received.

US005708849A

United States Patent [19]

Coke et al.

[11] Patent Number: 5,708,849

[45] Date of Patent: Jan. 13, 1998

[54] **IMPLEMENTING SCATTER/GATHER OPERATIONS IN A DIRECT MEMORY ACCESS DEVICE ON A PERSONAL COMPUTER**

[75] Inventors: James S. Coke, Cameron Park; Ajay V. Bhatt, Eldorado Hills; Stan Graham, Camaron Park; David Lent, Placerville, all of Calif.

[73] Assignee: Intel Corporation, Santa Clara, Calif.

[21] Appl. No.: 791,608

[22] Filed: Jan. 27, 1997

Related U.S. Application Data

[63] Continuation of Ser. No. 187,751, Jan. 26, 1994, abandoned.

[51] Int. Cl.[6] G06F 13/10

[52] U.S. Cl. 395/842; 395/310

[58] Field of Search 395/842, 843, 395/844, 845, 846, 847, 848, 310

[56] References Cited

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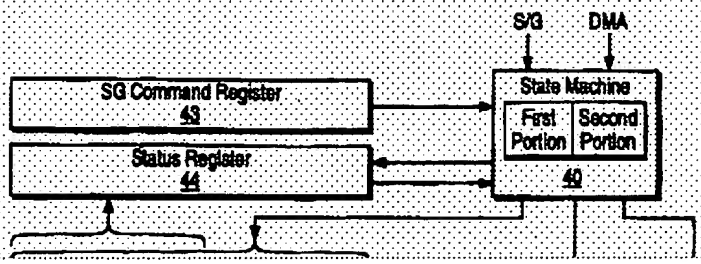
5,251,303	10/1993	Fogg, Jr. et al.	395/844
5,291,582	3/1994	Drako et al.	395/425
5,333,290	7/1994	Kato	395/846
5,333,294	7/1994	Schmidt	395/846
5,367,639	11/1994	Sodos	395/844

Primary Examiner—Eddie P. Chan
Assistant Examiner—Hiep T. Nguyen
Attorney, Agent, or Firm—Blakely, Sokoloff, Taylor & Zafman

[57] ABSTRACT

A direct memory access (DMA) circuit includes a first register for storing an address for the transfer of data, apparatus for transferring data at sequential addresses beginning at the address in the first register until all data at sequential addresses has been transferred, a second register for storing a beginning address for a list of addresses, and a state machine which responds to the completion of a transfer of data at sequential addresses beginning at the address in the first register and an indication that more data is to be transferred to transfer an address from the list at the address in the second register to the first register and causes the apparatus for transferring data to commence.

19 Claims, 5 Drawing Sheets



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Search Results - Record(s) 1 through 10 of 32 returned.

☐ 1. Document ID: US 20040123013 A1

L3: Entry 1 of 32 File: PGPB Jun 24, 2004

PGPUB-DOCUMENT-NUMBER: 20040123013
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040123013 A1

TITLE: Direct memory access controller system

PUBLICATION-DATE: June 24, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Clayton, Shawn Adam	Boylston	MA	US	
Fortin, Brian Mark	Hudson	MA	US	
Willie, Daniel Brian	Longmont	CO	US	
Wood, John Leland	Stratham	NH	US	

US-CL-CURRENT: 710/310; 710/308

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 20040073738 A1

L3: Entry 2 of 32 File: PGPB Apr 15, 2004

PGPUB-DOCUMENT-NUMBER: 20040073738
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040073738 A1

TITLE: Scalable efficient I/O port protocol

PUBLICATION-DATE: April 15, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kessler, Richard E.	Shrewsbury	MA	US	
Duncan, Samuel H.	Arlington	MA	US	
Hartwell, David W.	Bolton	MA	US	
Webb, David A.J. JR.	Groton	MA	US	
Lang, Steve	Stow	MA	US	

US-CL-CURRENT: 710/308; 711/147

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 20020166004 A1

L3: Entry 3 of 32 File: PGPB Nov 7, 2002

PGPUB-DOCUMENT-NUMBER: 20020166004
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020166004 A1

TITLE: Method for implementing soft-DMA (software based direct memory access engine) for multiple processor systems

PUBLICATION-DATE: November 7, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Kim, Jason Seung-Min	San Jose	CA	US	

US-CL-CURRENT: 710/22

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 20020161944 A1

L3: Entry 4 of 32 File: PGPB Oct 31, 2002

PGPUB-DOCUMENT-NUMBER: 20020161944
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20020161944 A1

TITLE: Programmable controller

PUBLICATION-DATE: October 31, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Okada, Kazunori	Kyoto		JP	

US-CL-CURRENT: 710/22

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 5. Document ID: US 6874054 B2

L3: Entry 5 of 32 File: USPT Mar 29, 2005

US-PAT-NO: 6874054
DOCUMENT-IDENTIFIER: US 6874054 B2

TITLE: Direct memory access controller system with message-based programming

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

☐ 6. Document ID: US 6865643 B2

L3: Entry 6 of 32 File: USPT Mar 8, 2005

US-PAT-NO: 6865643
DOCUMENT-IDENTIFIER: US 6865643 B2

TITLE: Communications architecture for a high throughput storage processor providing user data priority on shared channels

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 7. Document ID: US 6813689 B2

L3: Entry 7 of 32 File: USPT Nov 2, 2004

US-PAT-NO: 6813689
DOCUMENT-IDENTIFIER: US 6813689 B2

TITLE: Communications architecture for a high throughput storage processor employing extensive I/O parallelization

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 6792506 B2

L3: Entry 8 of 32 File: USPT Sep 14, 2004

US-PAT-NO: 6792506
DOCUMENT-IDENTIFIER: US 6792506 B2

TITLE: Memory architecture for a high throughput storage processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 6738836 B1

L3: Entry 9 of 32 File: USPT May 18, 2004

US-PAT-NO: 6738836
DOCUMENT-IDENTIFIER: US 6738836 B1

TITLE: Scalable efficient I/O port protocol

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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☐ 10. Document ID: US 6687796 B1

L3: Entry 10 of 32 File: USPT Feb 3, 2004

US-PAT-NO: 6687796
DOCUMENT-IDENTIFIER: US 6687796 B1

TITLE: Multi-channel DMA with request scheduling

Full | Title | Citation | Front | Review | Classification | Date | Reference | Claims | KWIC | Draw Desc | Image

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Terms	Documents
L1 and L2	32

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Search Results - Record(s) 11 through 20 of 32 returned.

11. Document ID: US 6502169 B1

L3: Entry 11 of 32 File: USPT Dec 31, 2002

US-PAT-NO: 6502169
DOCUMENT-IDENTIFIER: US 6502169 B1

TITLE: System and method for detection of disk storage blocks containing unique values

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

12. Document ID: US 6425053 B1

L3: Entry 12 of 32 File: USPT Jul 23, 2002

US-PAT-NO: 6425053
DOCUMENT-IDENTIFIER: US 6425053 B1

TITLE: System and method for zeroing data storage blocks in a raid storage implementation

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

13. Document ID: US 6363444 B1

L3: Entry 13 of 32 File: USPT Mar 26, 2002

US-PAT-NO: 6363444
DOCUMENT-IDENTIFIER: US 6363444 B1

TITLE: Slave processor to slave memory data transfer with master processor writing address to slave memory and providing control input to slave processor and slave memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

14. Document ID: US 6324598 B1

L3: Entry 14 of 32 File: USPT Nov 27, 2001

US-PAT-NO: 6324598
DOCUMENT-IDENTIFIER: US 6324598 B1

TITLE: Software enlarged tag register and method thereof for noting the completion of a DMA transfer within a chain of DMA transfers

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 15. Document ID: US 6122699 A

L3: Entry 15 of 32 File: USPT Sep 19, 2000

US-PAT-NO: 6122699
DOCUMENT-IDENTIFIER: US 6122699 A
**** See image for Certificate of Correction ****

TITLE: Data processing apparatus with bus intervention means for controlling interconnection of plural busses

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 16. Document ID: US 6006286 A

L3: Entry 16 of 32 File: USPT Dec 21, 1999

US-PAT-NO: 6006286
DOCUMENT-IDENTIFIER: US 6006286 A

TITLE: System for controlling data packet transfers by associating plurality of data packet transfer control instructions in packet control list including plurality of related logical functions

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 17. Document ID: US 5983301 A

L3: Entry 17 of 32 File: USPT Nov 9, 1999

US-PAT-NO: 5983301
DOCUMENT-IDENTIFIER: US 5983301 A

TITLE: Method and system for assigning a direct memory access priority in a packetized data communications interface device

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 18. Document ID: US 5948080 A

L3: Entry 18 of 32 File: USPT Sep 7, 1999

US-PAT-NO: 5948080
DOCUMENT-IDENTIFIER: US 5948080 A
**** See image for Certificate of Correction ****

TITLE: System for assigning a received data packet to a data communications channel by comparing portion of data packet to predetermined match set to check correspondence for directing channel select signal

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

19. Document ID: US 5933654 A

L3: Entry 19 of 32 File: USPT Aug 3, 1999

US-PAT-NO: 5933654
DOCUMENT-IDENTIFIER: US 5933654 A

TITLE: Dynamic buffer fracturing by a DMA controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

20. Document ID: US 5889480 A

L3: Entry 20 of 32 File: USPT Mar 30, 1999

US-PAT-NO: 5889480
DOCUMENT-IDENTIFIER: US 5889480 A

TITLE: Full duplex serial codec interface with DMA

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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Terms	Documents
L1 and L2	32

Display Format: - Change Format

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Hit List

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Search Results - Record(s) 21 through 30 of 32 returned.

☐ 21. Document ID: US 5881248 A

L3: Entry 21 of 32 File: USPT Mar 9, 1999

US-PAT-NO: 5881248
DOCUMENT-IDENTIFIER: US 5881248 A

TITLE: System and method for optimizing system bus bandwidth in an embedded communication system

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 22. Document ID: US 5878216 A

L3: Entry 22 of 32 File: USPT Mar 2, 1999

US-PAT-NO: 5878216
DOCUMENT-IDENTIFIER: US 5878216 A

TITLE: System and method for controlling a slave processor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 23. Document ID: US 5872940 A

L3: Entry 23 of 32 File: USPT Feb 16, 1999

US-PAT-NO: 5872940
DOCUMENT-IDENTIFIER: US 5872940 A

TITLE: Programmable read/write access signal and method therefor

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 24. Document ID: US 5852742 A

L3: Entry 24 of 32 File: USPT Dec 22, 1998

US-PAT-NO: 5852742
DOCUMENT-IDENTIFIER: US 5852742 A

TITLE: Configurable data processing pipeline

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 25. Document ID: US 5835788 A

L3: Entry 25 of 32 File: USPT Nov 10, 1998

US-PAT-NO: 5835788
DOCUMENT-IDENTIFIER: US 5835788 A

TITLE: System for transferring input/output data independently through an input/output bus interface in response to programmable instructions stored in a program memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 26. Document ID: US 5818029 A

L3: Entry 26 of 32 File: USPT Oct 6, 1998

US-PAT-NO: 5818029
DOCUMENT-IDENTIFIER: US 5818029 A

TITLE: Method and apparatus for connecting PCMCIA cards to computer interfaces

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 27. Document ID: US 5812876 A

L3: Entry 27 of 32 File: USPT Sep 22, 1998

US-PAT-NO: 5812876
DOCUMENT-IDENTIFIER: US 5812876 A

TITLE: DMA controller which can be controlled by host and local processors

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 28. Document ID: US 5809334 A

L3: Entry 28 of 32 File: USPT Sep 15, 1998

US-PAT-NO: 5809334
DOCUMENT-IDENTIFIER: US 5809334 A

TITLE: Receive packet pre-parsing by a DMA controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

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☐ 29. Document ID: US 5802327 A

L3: Entry 29 of 32 File: USPT Sep 1, 1998

US-PAT-NO: 5802327
DOCUMENT-IDENTIFIER: US 5802327 A

TITLE: Device for SCSI expansion

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

☐ 30. Document ID: US 5598579 A

L3: Entry 30 of 32 File: USPT Jan 28, 1997

US-PAT-NO: 5598579
DOCUMENT-IDENTIFIER: US 5598579 A

TITLE: System fpr transferring data between two buses using control registers writable by host processor connected to system bus and local processor coupled to local bus

Full | Title | Citation | Front | Review | Classification | Date | Reference | | | Claims | KWIC | Draw Desc | Image

Clear | Generate Collection | Print | Fwd Refs | Bkwd Refs | Generate OACS

Terms	Documents
L1 and L2	32

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L3: Entry 32 of 32 File: USPT May 30, 1995

US-PAT-NO: 5420984
DOCUMENT-IDENTIFIER: US 5420984 A
** See image for Certificate of Correction **

TITLE: Apparatus and method for rapid switching between control of first and second DMA circuitry to effect rapid switching beween DMA communications

DATE-ISSUED: May 30, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Good; Christopher J.	St. Briavels			GB
Nordman; Joseph M.	West Bend	WI		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Genroco, Inc.	Slinger	WI			02

APPL-NO: 08/ 106186 [PALM]
DATE FILED: August 13, 1993

PARENT-CASE:
This application is a continuation of application Ser. No. 07/906,911, filed Jun. 30, 1992, now abandoned.

INT-CL: [06] G06 F 3/00

US-CL-ISSUED: 395/275; 395/250, 395/425, 364/242.31, 364/DIG.1
US-CL-CURRENT: 710/22; 709/212, 710/27, 710/28

FIELD-OF-SEARCH: 395/250, 395/278, 395/425, 364/200

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL | Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4032899	June 1977	Jenny et al.	364/200
☐	4246637	January 1981	Brown et al.	364/200
☐	4298954	November 1981	Bigelow	364/900
☐	4475155	October 1984	Oishi et al.	364/200
☐	4571674	February 1986	Hartung	364/200
	4819203	April 1989	Shiroyanagi et al.	364/900

☐	4965801	October 1990	DuLac	371/40.1
☐	5150465	September 1992	Bush et al.	395/275
☐	5193149	March 1993	Awiszio et al.	395/200
☐	5195089	March 1993	Sindhu et al.	370/85.1
☐	5276842	January 1994	Sugita	395/425
☐	5297260	March 1994	Kametani	395/325

ART-UNIT: 237

PRIMARY-EXAMINER: Shin; Christopher B.

ATTY-AGENT-FIRM: Quarles & Brady

ABSTRACT:

A method and apparatus for improving sustainable data throughput between a host system minicomputer and a plurality of peripheral memories utilizes a dual-ported RAM memory, a microelectronic processor with an instruction rate of 10 MIPS or greater and task switching firmware executed by the microelectronic processor for rapid switching between communication on a peripheral data bus to the peripheral memories and communication on a system data bus having a relatively higher data rate. Also disclosed is a method of data caching on the host system using the peripheral controller.

6 Claims, 3 Drawing figures

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